REMARKS

Claims 45-67 are pending in the present application.

In the office action mailed July 9, 2004 (the "Office Action"), the drawings were objected to for failing to comply with 37 C.F.R. 1.84(p)(5). Additionally, claims 45-67 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-44 of U.S. Patent No. 6,735,103 to Kirsch (the "Kirsch patent").

As noted in the Office Action by the Examiner, claims 1-44 are withdrawn from consideration. Claims 2-44, however, were *cancelled* in a preliminary amendment included with the filing of the present application (the "first preliminary amendment"), and claim 1 was *cancelled* in a supplemental preliminary amendment submitted June 2, 2004 (the "second preliminary amendment"). Copies of the first and second preliminary amendments have been included with this response for reference by the Examiner. Acknowledgement by the Examiner of the cancellation of claims 1-44 is requested.

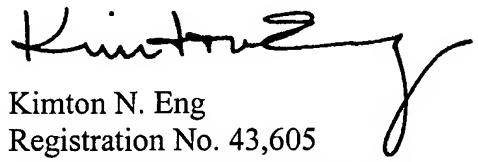
Additionally, the Examiner's objection to the drawings should have been resolved by amendments to the specification made in the first preliminary amendment. In the first preliminary amendment the specification was amended to delete the reference to "112" in the paragraph beginning on page 1, line 9, and reference to "an active circuit 339" was added to the paragraph beginning on page 8, line 18. These amendments directly address the Examiner's objection to the drawings, and consequently, the objections should be withdrawn.

With respect to the rejection of claims 45-67 under the judicially created doctrine of obviousness-type double patenting, a timely filed terminal disclaimer in compliance with 37 C.F.R. 1.321(c) has been provided with this amendment. Consequently, the rejection of claims 45-67 for obviousness-type double patenting should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Enclosures:
- Postcard
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- Fee Transmittal Sheet (+ copy)
- Copy of First Preliminary Amendment
- Copy of Second Preliminary Amendment
- Terminal Disclaimer

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EXPRESS MAIL NO. EL990359598US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicant : Howard C. Kirsch
Attorney Docket No. : 501214.02 (30204/US/2)
Filed : Concurrently herewith
Customer No. : 27,076
Title : SYSTEM AND METHOD TO AVOID VOLTAGE READ ERRORS IN OPEN DIGIT LINE ARRAY DYNAMIC RANDOM ACCESS MEMORIES

Prior Application:

Examiner : Trong Q. Phan
Art Unit : 2818
Serial No. : 10/231,680

PRELIMINARY AMENDMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Amendments to the Drawings begin on page 5 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Amendments to the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 10/231,680, filed August 29, 2002. --

Please replace the paragraph beginning on page 1, line 9 with the following amended paragraph:

As is well known in the art and shown in Figure 1, a DRAM cell 100 typically comprise a capacitor 104 and access transistor 108 pair. One plate of the capacitor 104 is connected to a common cell plate (not shown) to which all capacitors in that DRAM cell array are connected, a subset of which ~~112~~ is shown in Figure 1. The other plate of the capacitor 104 is coupled to a drain of the access transistor 108. The gate of the access transistor 108 is connected to a word line 116 which allows all the DRAM cells coupled to each word line 116 to be activated, while the source of the access transistor 108 is coupled to a digit line 120 which the DRAM cell 100 will read from and write to during memory operations. Activating the gate of the access transistor allows a high voltage charge (Vcc) or low voltage charge (ground) carried by the digit line 120 to pass to the capacitor 104, thus writing the voltage of the digit line 120 to the capacitor 104.

Please replace the paragraph beginning on page 8, line 18 with the following amended paragraph:

Added to this system is a selective cell plate coupling transistor 330 which is coupled to a controller 332. The transistor 330 has one of its terminals coupled through signal line 334 to all of the odd-numbered sub-arrays 302 and the other of its terminals coupled through signal line 336 to all of the even-numbered sub-arrays 302. The controller 332 receives signals generated by other circuitry in a DRAM providing an indication of when a memory read operation is to occur, such as from a row active line 337. For example, as shown in Figure 3A, an active circuit 339 is coupled to the sub-arrays 302 for activation thereof, and is further

coupled to the controller 332 to provide a signal to the controller 332 via the row active line 337 that is indicative of when a memory operation is to occur. The controller 332 normally applies a signal to the gate of the transistor 330 to turn ON the transistor 330. The transistor 330 and signal lines 334, 336 then couple the cell plates 310 of all of the odd-numbered sub-arrays 302 to the cell plates 310 of all of the even-numbered sub-arrays 302. Thus, in this condition, the cell plates of adjacent sub-arrays 302 are coupled to each other. A $V_{CC}/2$ generator 338 is coupled to the signal line 336 to bias the cell plates 310 of the even sub-arrays 302 to $V_{CC}/2$. Of course, when the transistor 330 is ON, the $V_{CC}/2$ generator 338 is also coupled to the signal line 334 to bias the cell plates 310 of the odd sub-arrays 302 to $V_{CC}/2$. The large capacitance of the cell plates 310 allows the voltage of the cell plates 310 for the odd-numbered sub-arrays 302 to remain essentially constant at $V_{CC}/2$.

Amendments to the Claims:

Please cancel claims 2-44

Listing of Claims:

1. (Original) A voltage reading enhancement system for an open digit line array DRAM device comprising a plurality of sub-arrays, the voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to decouple the component in the active sub-array from the corresponding component in the reference sub-array when the active row signal is received.

2-44. (Cancelled)

Amendments to the Drawings:

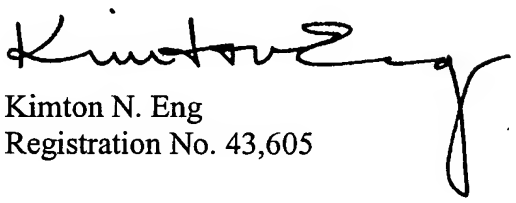
The attached sheets of drawings includes changes to Figures 3A, 3B, and 4.

Also attached are replacement formal drawings, Figures 1-5.

Attachments: Replacement Sheets
Annotated Sheet Showing Changes

Respectfully submitted,

DORSEY & WHITNEY LLP



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H:\IP\Documents\Clients\Micron Technology\1200\501214.02\501214.02 prelim amend with appl.doc

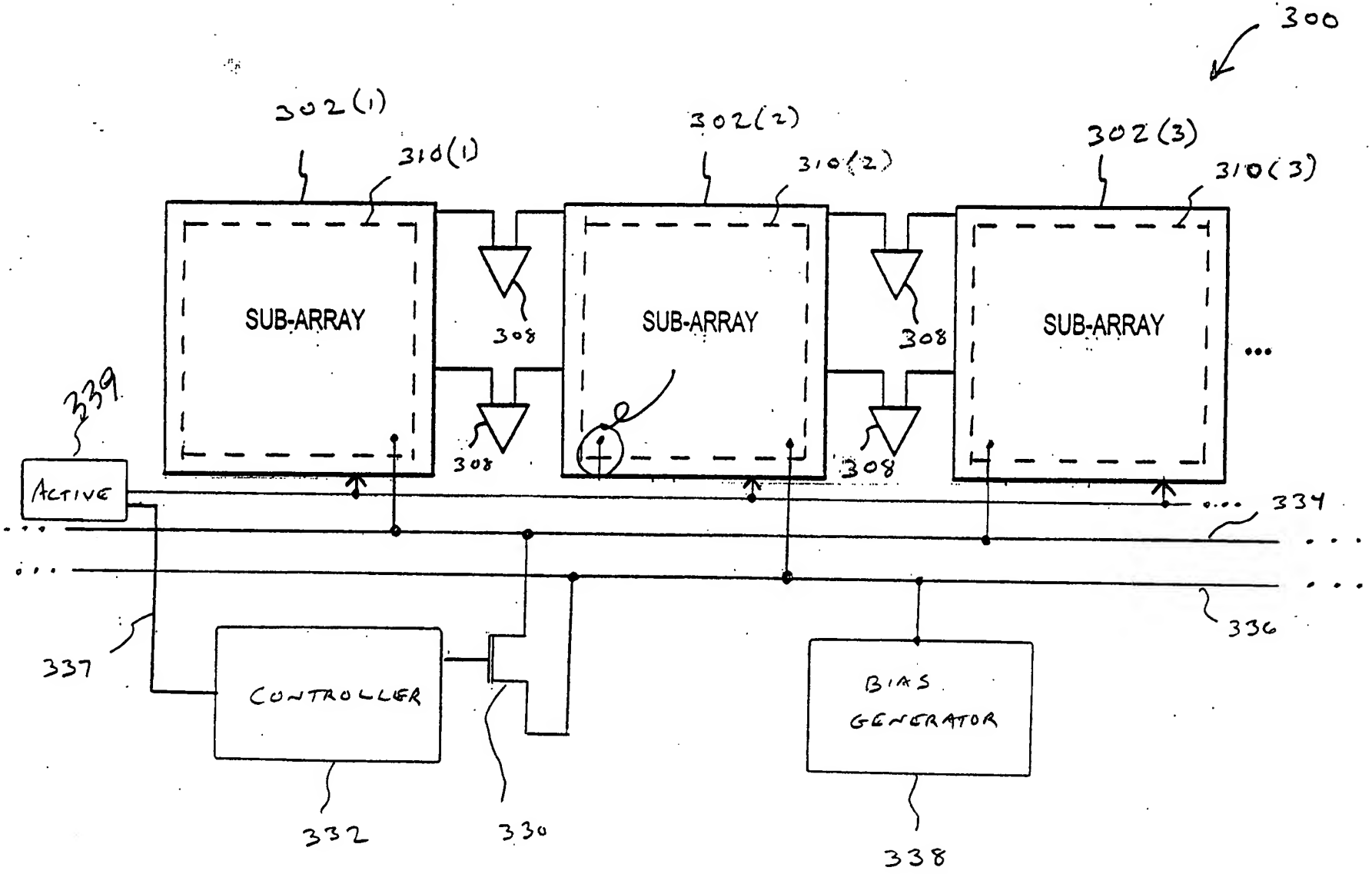


FIGURE 3A

Annotated Sheet Showing Changes

Annotated Sheet
Showing Changes

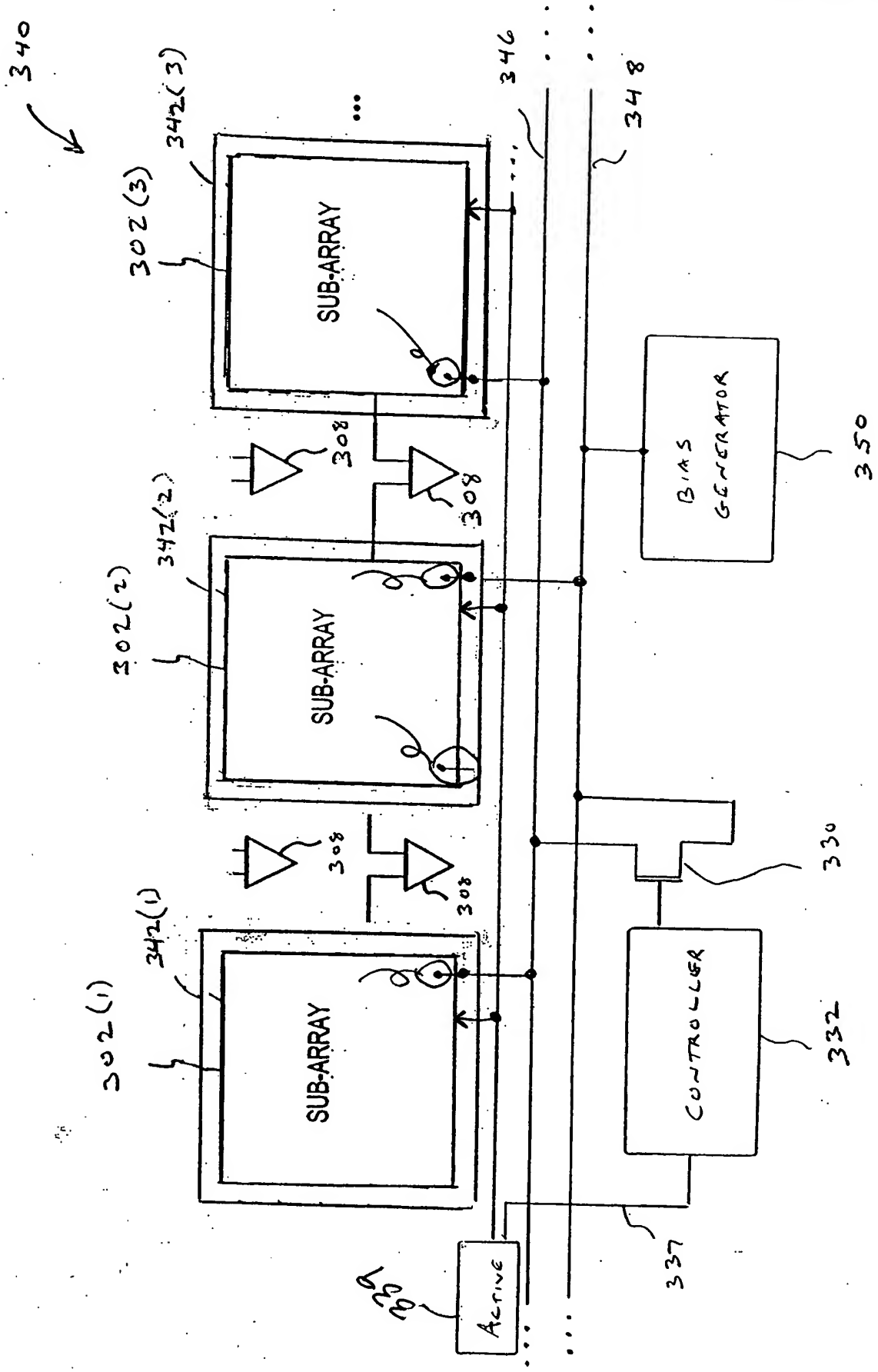


FIGURE 3B

Annotated Sheet
Showing Changes

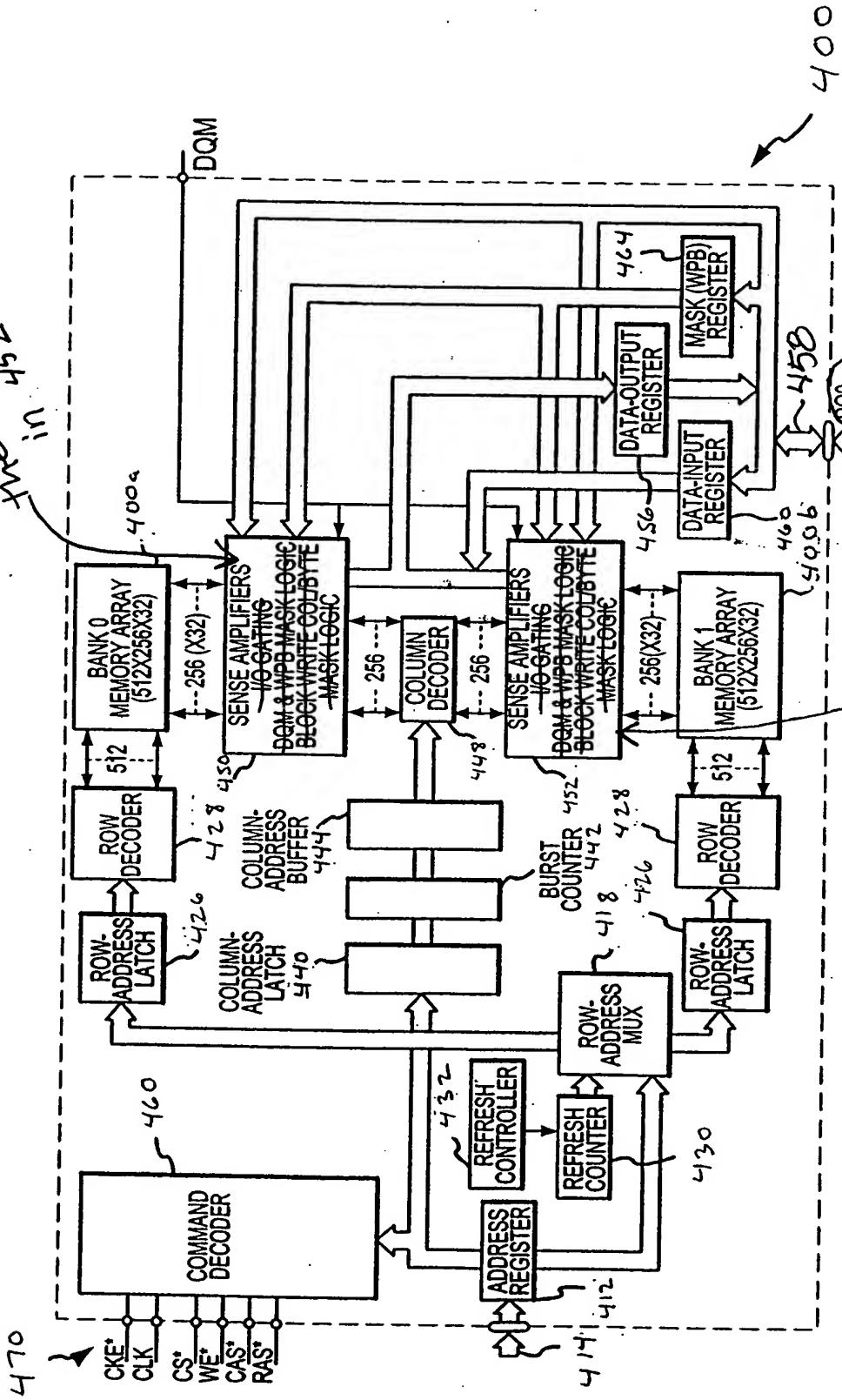


FIG. 4

should read same as the 457 in

should read: "SENSE AMPLIFIERS + ASSOCIATED COLUMN CIRCUITRY"

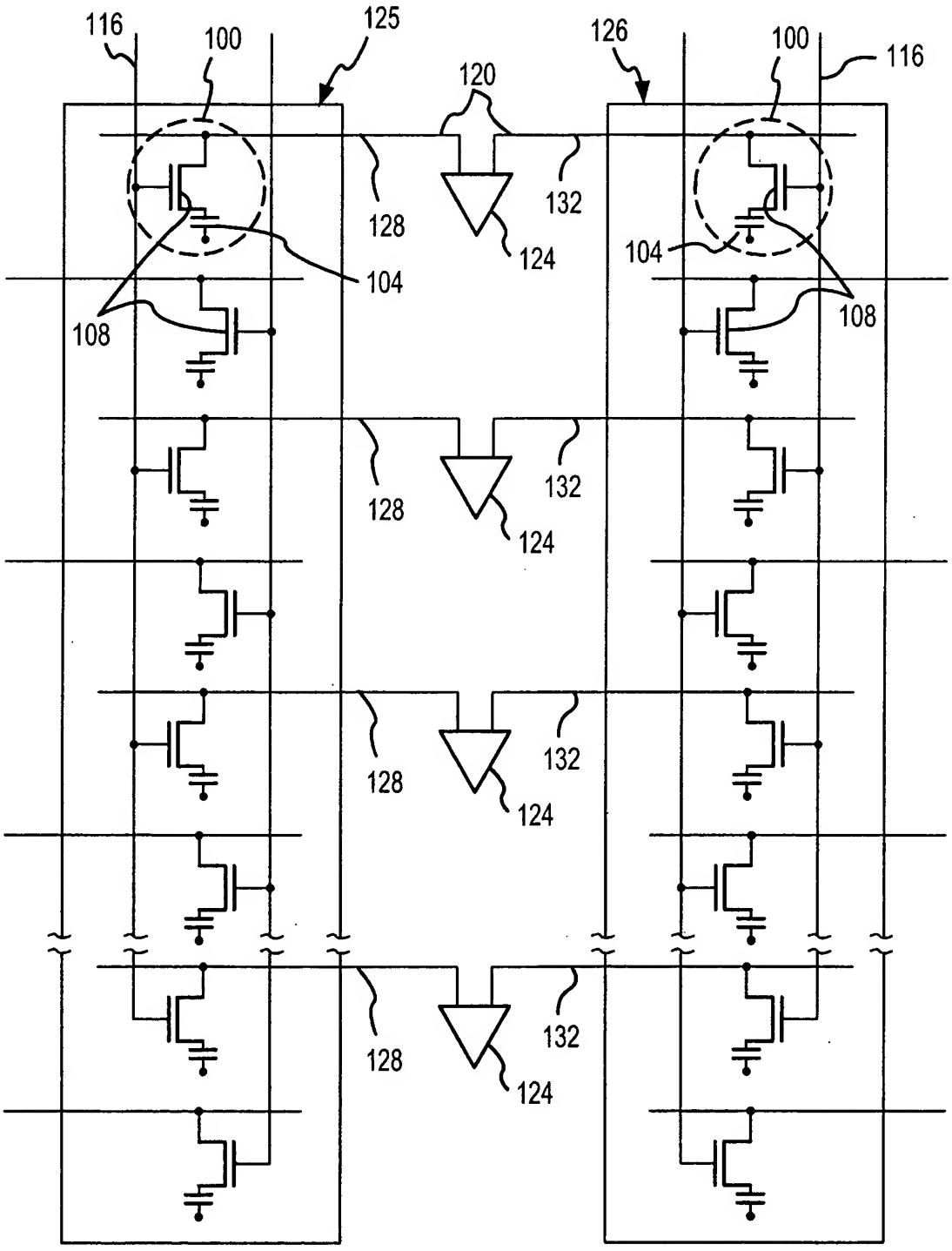
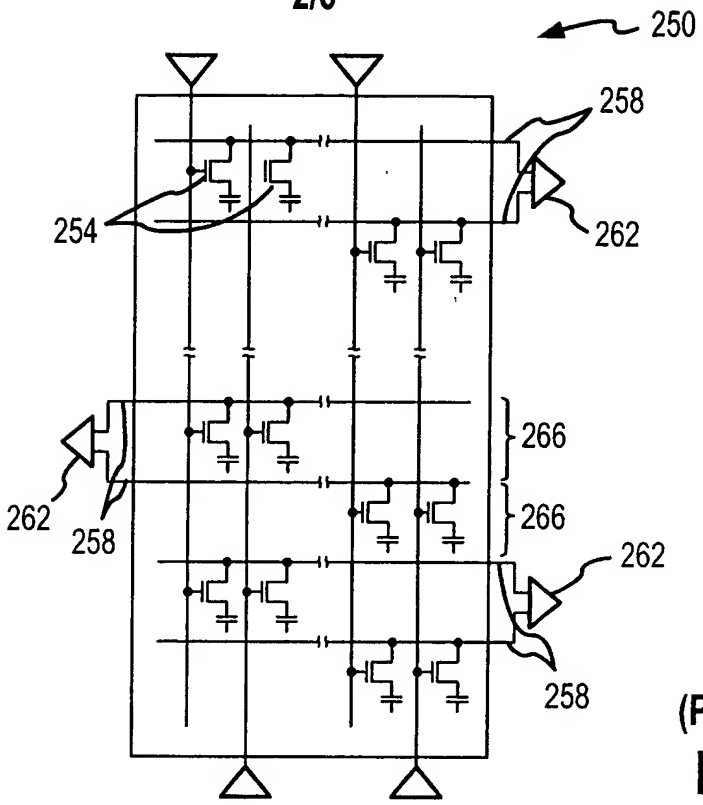


FIG.1
(PRIOR ART)



(PRIOR ART)

FIG.2A

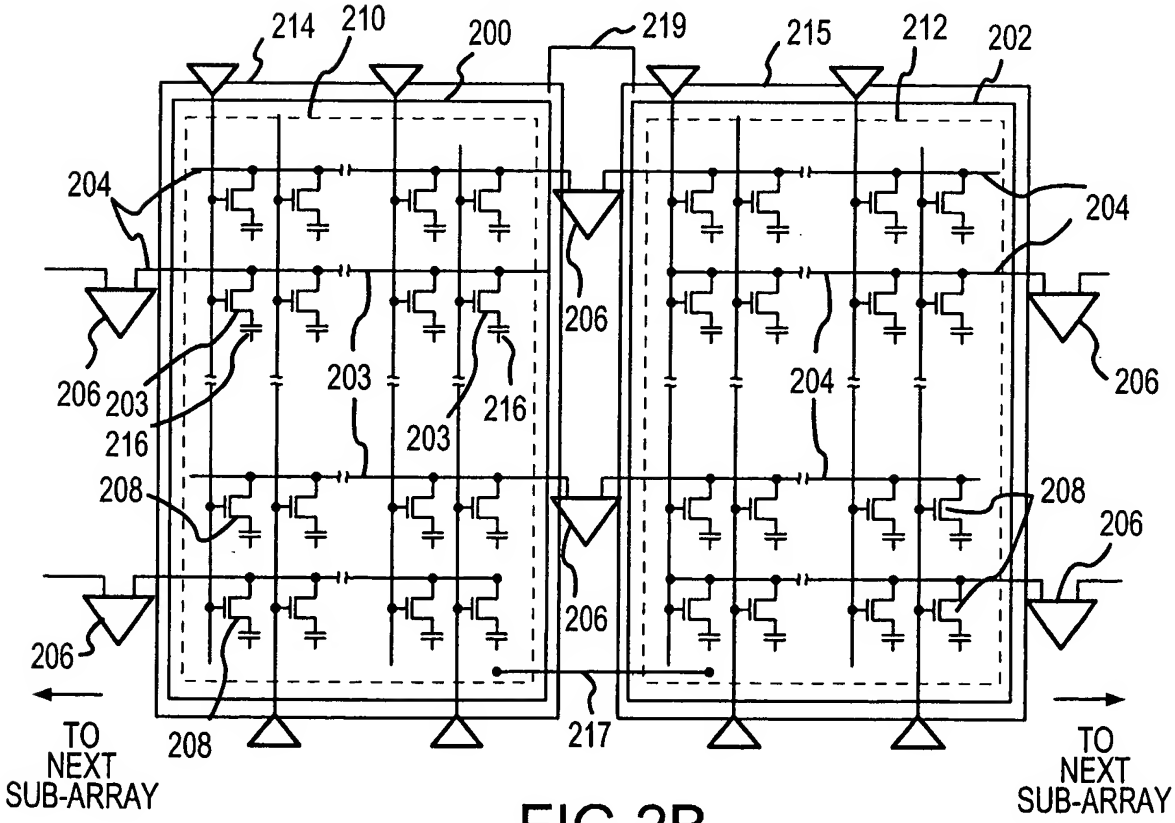


FIG.2B

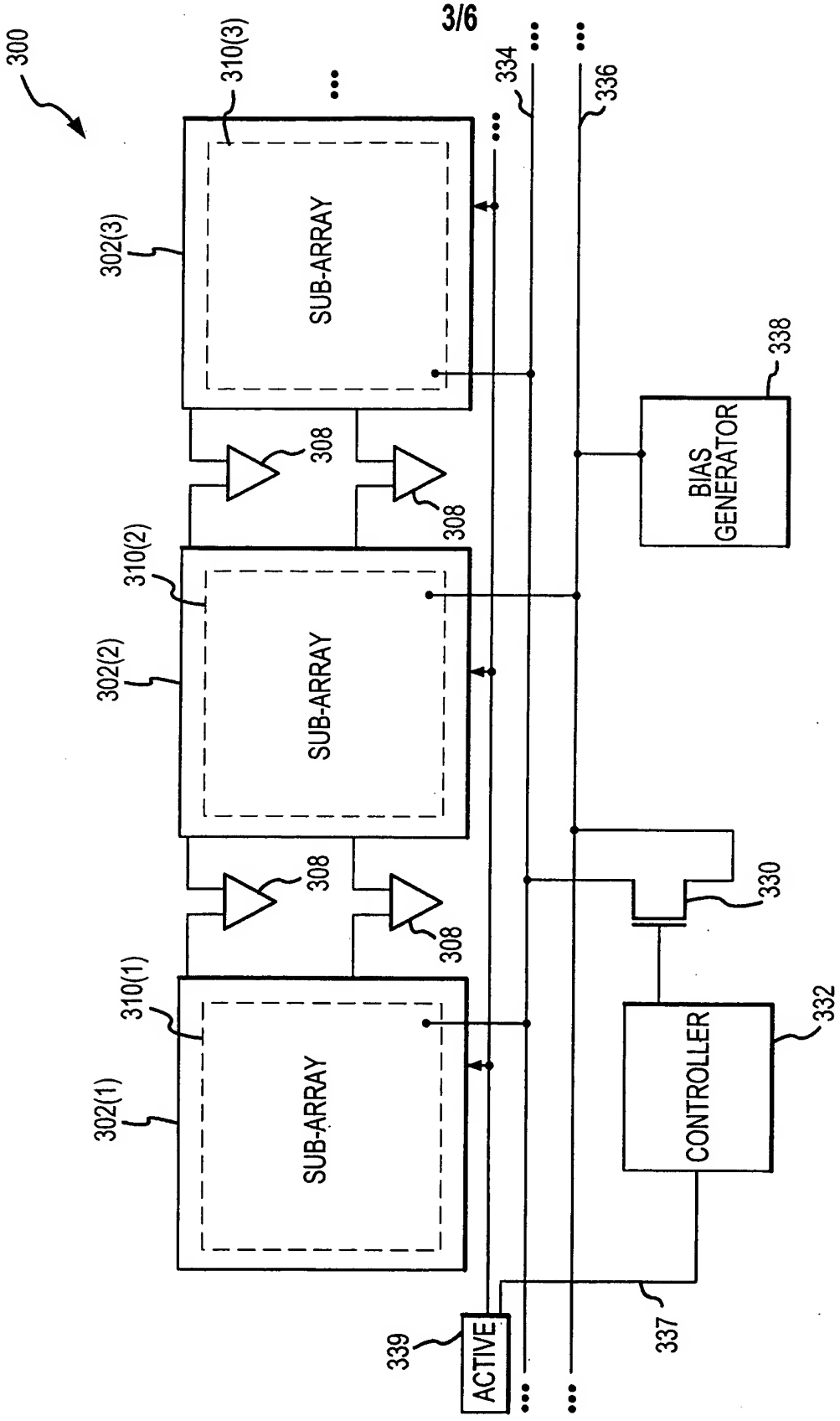

300
310(3)
302(3)
SUB-ARRAY
334
336
338
BIAS GENERATOR
308
310(2)
302(2)
SUB-ARRAY
330
310(1)
302(1)
SUB-ARRAY
CONTROLLER
332
339
ACTIVE
337

FIG.3A

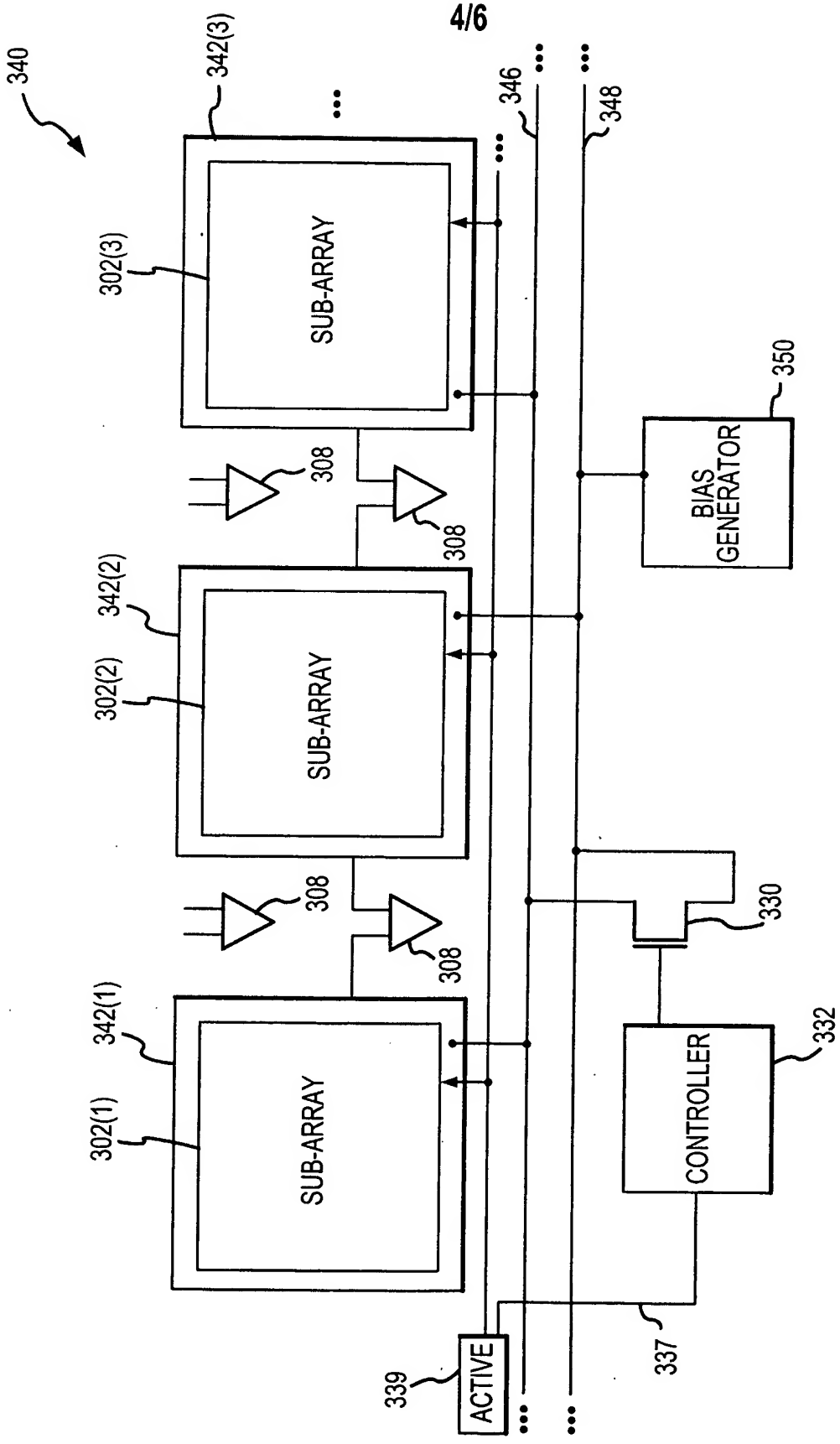

340
342(3)
346
348
302(3)
SUB-ARRAY
308
308
350
BIAS GENERATOR
342(2)
302(2)
SUB-ARRAY
308
308
330
342(1)
302(1)
SUB-ARRAY
CONTROLLER
332
339
ACTIVE
337

FIG.3B

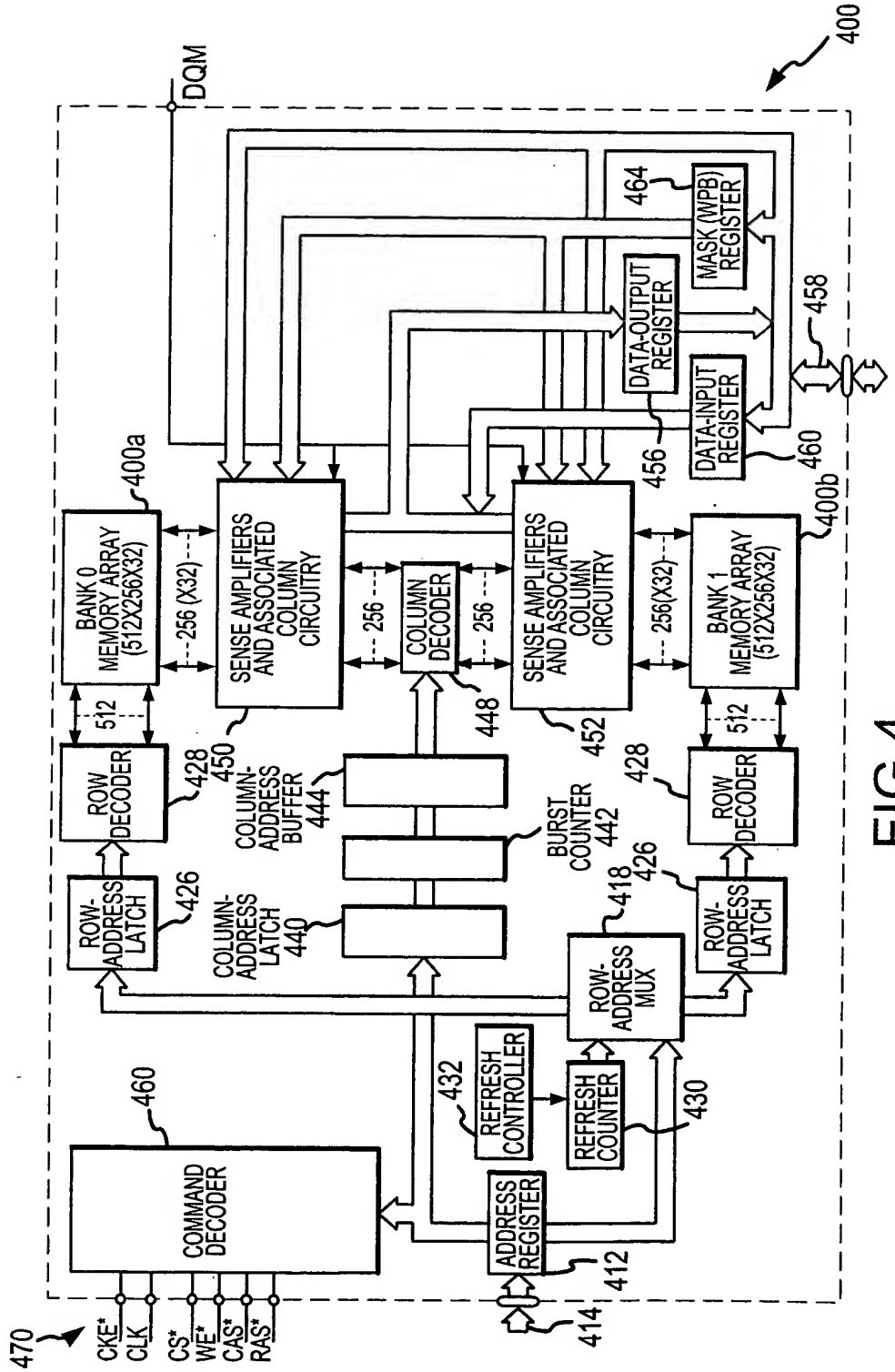

400
DQM
464
MASK (WPB) REGISTER
458
DATA-OUTPUT REGISTER
DATA-INPUT REGISTER
456
460
400a
400b
BANK 0 MEMORY ARRAY (512X256X32)
256 (X32)
SENSE AMPLIFIERS AND ASSOCIATED COLUMN CIRCUITRY
256
COLUMN DECODER
448
452
BANK 1 MEMORY ARRAY (512X256X32)
512
ROW DECODER
428
450
COLUMN-ADDRESS BUFFER 444
BURST COUNTER 442
ROW-ADDRESS LATCH
426
COLUMN-ADDRESS LATCH 440
418
ROW-ADDRESS MUX
REFRESH CONTROLLER
432
REFRESH COUNTER
430
COMMAND DECODER
ADDRESS REGISTER
412
414
470
CKE*
CLK
CS*
WE*
CAS*
RAS*

FIG.4

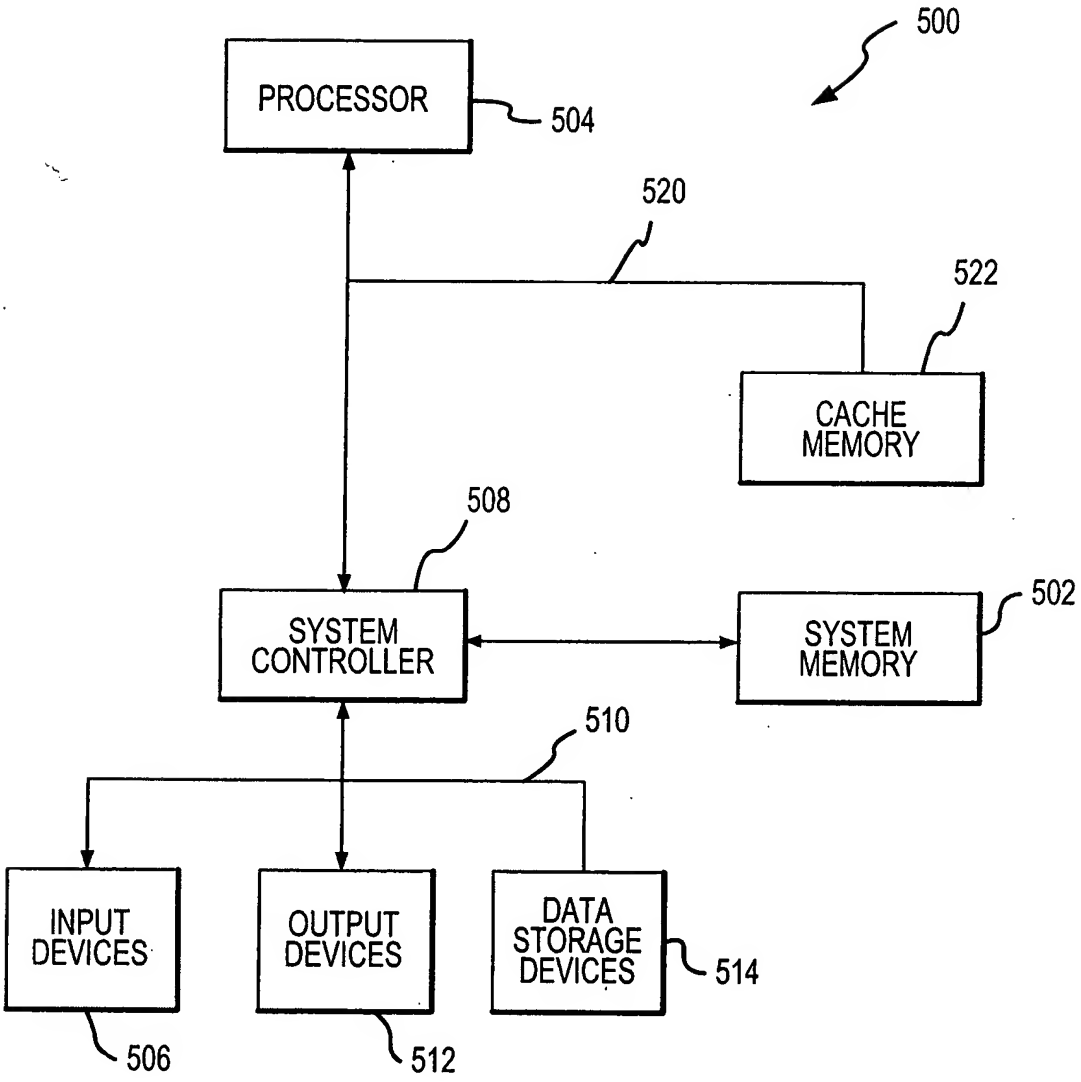

500
PROCESSOR
504
520
522
CACHE MEMORY
508
SYSTEM CONTROLLER
SYSTEM MEMORY
502
510
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE DEVICES
514
506
512

FIG.5

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 2, 2004
Date

Ayesha J. Shaikh

COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/815,890	Confirmation No.	: Not Yet Assigned
Applicant	: Howard C. Kirsch		
Filed	: March 30, 2004	Attorney Docket No.	: 501214.02 (30204/US/2)
Art Unit	: Not Yet Assigned	Customer No.	: 27,076
Examiner	: Not Yet Assigned		
Title	: SYSTEM AND METHOD TO AVOID VOLTAGE READ ERRORS IN OPEN DIGIT LINE ARRAY DYNAMIC RANDOM ACCESS MEMORIES		

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 45-67, as follows:

Listing of Claims:

1-44. (Cancelled)

45. (New) A memory device, comprising:

a first memory array having a cell plate and memory cells;

a second memory array having a cell plate and memory cells;

a plurality of sense amplifiers, each coupled to a respective first digit line coupled to memory cells of the first memory array and further coupled to a respective second digit line coupled to memory cells of the second memory array;

a switch coupled to the cell plate of the first memory array and further coupled to the cell plate of the second memory array to electrically couple the cell plates of the respective memory arrays; the switch adapted to decouple the cell plates of the first and second memory arrays in response to an inactive balance signal; and

a control circuit coupled to the switch and adapted to generate an inactive balance signal when accessing a memory cell of the first or second memory array.

46. (New) The memory device of claim 45 wherein the first and second arrays are located adjacent to one another.

47. (New) The memory device of claim 45, further comprising a bias generator coupled to the cell plates of the first and second memory arrays to bias the cell plates to a reference voltage level.

48. (New) The memory device of claim 47 wherein the bias generator comprises a voltage generator adapted to generate an output voltage having a voltage level approximately half of a supply voltage level.

49. (New) The memory device of claim 45 wherein the switch coupled to the cell plates of the first and second memory arrays comprises a transistor having a first terminal coupled to the cell plate of the first memory array, a second terminal coupled to the cell plate of the second memory array, and a control terminal coupled to the control circuit.

50. (New) A memory device, comprising:

a first memory array formed in a first region of a substrate, the first memory array having memory cells;

a second memory array formed in a second region of the substrate, the second memory array having memory cells;

a plurality of sense amplifiers, each coupled to a respective first digit line coupled to memory cells of the first memory array and further coupled to a respective second digit line coupled to memory cells of the second memory array;

a switch coupled to the first region of the substrate and further coupled to the second region of the substrate to electrically couple the regions of the substrate of the respective memory arrays; the switch adapted to decouple the first and second regions of the substrate in response to an inactive balance signal; and

a control circuit coupled to the switch and adapted to generate an inactive balance signal when accessing a memory cell of the first or second memory array.

51. (New) The memory device of claim 50 wherein the first and second arrays are formed adjacent to one another.

52. (New) The memory device of claim 50, further comprising a bias generator coupled to the first and second regions of the substrate to bias the first and second regions to a reference voltage level.

53. (New) The memory device of claim 52 wherein the bias generator comprises a voltage generator adapted to generate an negative output voltage.

54. (New) The memory device of claim 50 wherein the switch coupled to the first and second regions of the substrate comprises a transistor having a first terminal coupled to the first region of the substrate, a second terminal coupled to the second region of the substrate, and a control terminal coupled to the control circuit.

55. (New) A memory device, comprising:

a first plurality of memory cell arrays, the first plurality having at least one cell plate for the memory cell arrays;

a second plurality of memory cell arrays, the second plurality having at least one cell plate for the memory cell arrays; the memory cell arrays of the first plurality located adjacent the memory cell arrays of the second plurality;

a plurality of sets of sense amplifiers, each set of sense amplifiers having sense amplifiers coupled to respective pairs of digit lines, a first digit line of each pair coupled to memory cells of a memory cell array in the first plurality of memory cell arrays and a second digit line of each pair coupled to memory cells of a memory cell array of the second plurality of memory cell arrays;

a switch coupled to the cell plate of the first plurality of memory cell arrays and further coupled to the cell plate of the second plurality of memory cell arrays to electrically couple together the cell plates of the first and second pluralities in response to an active switch signal and decouple the cell plates of the first and second pluralities in response to an inactive switch signal; and

a control circuit coupled to the switch and adapted to generate an active switch signal prior to initiation of a memory access operation to memory cells of the first plurality of memory cell arrays or memory cells of the second plurality of memory cell arrays and generate an inactive switch signal in response to the initiation of a memory access operation.

56. (New) The memory device of claim 55 wherein the first plurality of memory cell arrays are formed in a first region of a substrate and the second plurality of memory cell arrays are formed in a second region of the substrate, and the memory device comprises a second switch coupled to the first and second regions of the substrate to electrically couple together the first and second regions in response to an active switch signal and decouple the first and second regions in response to an inactive switch signal.

57. (New) The memory device of claim 55, further comprising a bias generator coupled to the cell plates of the first plurality of memory cell arrays and further coupled to the cell plates of the second plurality of memory cell arrays to bias the cell plates to a reference voltage level.

58. (New) The memory device of claim 57 wherein the bias generator comprises a voltage generator adapted to generate an output voltage having a voltage level approximately half of a supply voltage level.

59. (New) The memory device of claim 55 wherein the switch coupled to the cell plates of the first and second plurality of memory cell arrays comprises a transistor having a first terminal coupled to the cell plate of the first plurality of memory cell arrays, a second terminal coupled to the cell plate of the second plurality of memory cell arrays, and a control terminal coupled to the control circuit.

60. (New) A method for accessing dynamic random access memory cells, comprising:

biasing cell plates of adjacent memory cell arrays to a reference voltage level;

coupling the cell plates of the adjacent memory cell arrays prior to initiation of a memory access operation to a memory cell in either of the adjacent memory cell arrays;

decoupling the cell plates of the adjacent memory cell arrays in response to initiation of the memory access operation to a memory cell in either of the adjacent memory cell arrays; and

sensing a voltage differential between the accessed memory cell and the cell plate of the memory cell array in which the accessed memory cell is not located.

61. (New) The method of claim 60, further comprising

coupling respective regions of a substrate in which in which the adjacent memory cell arrays are formed prior to initiation of a memory access operation to a memory cell in either of the adjacent memory cell arrays; and

decoupling the respective regions of the substrate of the adjacent memory cell arrays in response to initiation of the memory access operation to a memory cell in either of the adjacent memory cell arrays.

62. (New) The method of claim 60 wherein biasing the cell plates of adjacent memory cell arrays comprises biasing the cell plates of adjacent memory cell arrays to a voltage level approximately half of a supply voltage level.

63. (New) The method of claim 60 wherein sensing a voltage differential between the accessed memory cell and the cell plate of the memory cell array in which the accessed memory cell is not located comprises activating a sense amplifier having an open digit line architecture coupled to a first digit line coupled to memory cells of one of the memory cell arrays and further coupled to a second digit line coupled to memory cells of the other memory cell array.

64. (New) A method for accessing dynamic random access memory, comprising:

electrically coupling together cell plates of first and second memory cell arrays;

decoupling the cell plates of the first and second memory cell arrays;

activating a row of memory cells in the first memory cell array; and

for at least one memory cell of the activated row, comparing a voltage resulting from activation of the row of memory cells and a reference voltage of the second memory cell array.

65. (New) The method of claim 64, further comprising biasing the cell plates of the first and second memory cell arrays to the reference voltage prior to decoupling the cell plates of the first and second memory cell arrays.

66. (New) The method of claim 65 wherein biasing the cell plates of the first and second memory cell arrays comprises biasing the cell plates of adjacent memory cell arrays to a voltage level approximately half of a supply voltage level.

67. (New) The method of claim 64, further comprising:

electrically coupling together respective regions of a substrate in which the first and second memory cell arrays are formed; and

decoupling the respective regions of the substrate in which the first and second memory cell arrays are formed prior to activating a row of memory cells in the first memory cell array.

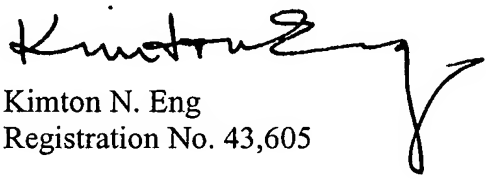
REMARKS

Claims 45-67 are pending in the present application. Claim 1 has been cancelled and claims 45-67 have been added by preliminary amendment. Claims 45-67 have been added to claim alternative embodiments of the invention described in the specification. Support for the subject matter of claims 45-67 can be found in the specification, including the figures and originally filed claims. No new matter has been added by claims 45-67.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance is earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Registration No. 43,605

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(206) 903-8820 (fax)

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